Nonvolatile memory based on sol-gel ZnO thin-film transistors with Ag nanoparticles embedded in the ZnO/gate insulator interface

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A nonvolatile memory is demonstrated using a solution-processed sol-gel ZnO thin-film transistor (TFT) in which Ag nanoparticles are embedded as charge storage nodes at the insulator-ZnO interface. Its TFT transfer characteristics exhibit a large clockwise hysteresis that is proportional to the gate bias sweep range. Measurement of the threshold voltage shift versus the pulse width of gate bias reveals that the device can be programed or erased at a time scale of as short as $10^{-3}$ s. Retention of the initial memory window is measured to be 27% after $10^5$ s and projected to last until $10^7$ s. © 2008 American Institute of Physics. [DOI: 10.1063/1.3041777]

Reprogramable nonvolatile memory is an indispensable element in most of the modern electronic devices. While Si-based technologies are still holding the largest share of nonvolatile memory devices, a demand for an alternative memory technology is rapidly growing especially in emerging applications such as radio frequency identification tags,1 where the conventional wafer technologies are too expensive or incompatible with the form-factor requirements such as bendability or flexibility. In these respects, memories based on organic thin-film transistors (TFTs) have been investigated as potential low-cost alternatives with a variety of fabrication routes and flexibility in choice of substrates.1,2 However, challenges still remain in developing inexpensive encapsulation layers to protect organic devices from oxygen and moisture.3 Another technology that is attracting a growing attention with the same motivations as organic technology is the TFTs based on oxide semiconductors such as ZnO and related compounds.4,5 Current development of ZnO-TFTs is mainly driven by the need for reliable and scalable TFT technologies with a performance compatible with Si-based technologies with a performance compatible with Si-based technologies, another technology typically used in metal-oxide-semiconductor field-effect transistor (MOSFET) memory devices is based on isolated nanoscale objects such as metal/semiconductor nanoparticles (NPs)9–11 or nanotubes12 that are embedded into gate insulators. Such nano-objects function as the charge storage nodes that trap or detract charges depending on the applied gate bias and thus effectively shift the threshold voltage, which in turn results in hysteresis in the transfer characteristics. This kind of scheme is popular because it can be used with well-established gate insulators and because some of the memory properties are controllable by NP density or multilayered NP layer configuration, etc.13 From the perspectives of low-cost processing, it would also be highly beneficial if major processes can be done using a solution process so that electronic devices can eventually be made by printing. Here we demonstrate reprogramable nonvolatile memory devices by solution-processing of sol-gel ZnO as semiconducting layers and Ag-NPs as charge storage nodes in TFT geometry, where Ag-NPs are embedded into the interface between ZnO channels and gate insulators.

Figure 1(a) shows the schematic structure of the ZnO/Ag-NP memory TFT under study. The memory TFT was fabricated on the heavily doped n-type (100) Si wafers having a 100 nm thick thermally grown SiO2 gate dielectric. Here the Si acts also as the back-gate electrode. A stable dispersion of Ag-NPs was prepared by mixing AgNO3 (0.03M) and polyvinyl pyrollidine (PVP) (0.003M) in dimethylformamide (DMF). Here PVP and DMF act as a stabilizing agent and reducing agent for the silver salt, respectively.14 A solution of ZnO precursor was prepared

Figure 1. (Color online) (a) Schematic of the ZnO/Ag-NP memory TFT and (b) SEM image of the Ag NPs on SiO2 surface after removing the organics by heating. (c) Cross-sectional HRTEM image of the fabricated device featuring Ag-NPs embedded at the SiO2-ZnO interface.
memory devices of ZnO-Ag NP TFTs, the transfer characteristics were measured for the various sweep ranges of gate voltage $V_{GS}$ in both forward ($-V_{GO}$ to $+V_{GO}$) and reverse ($+V_{GO}$ to $-V_{GO}$) directions, at a drain voltage ($V_{DS}$) of 3 V, as shown in Fig. 2(b). A clear clockwise hysteresis characterized by the positive hysteresis window $\Delta V_{T(hys)}$ (= $V_{T(\text{reverse})}$ – $V_{T(\text{forward})}$) is found for all the sweep ranges tried, which is attributed to the electron/hole trapping in the Ag-NPs during the positive/negative voltage sweep. Comparing with the reference device with no Ag-NPs that exhibits a low $\Delta V_{T}$ of only 1.5 V [see Fig. 2(c)], the device with Ag-NPs shows the relatively large $\Delta V_{T}$ up to 28.5 V at $V_{GO}$ of 50 V, confirming that the presented memory TFT operates through the electrostatic charging and discharging of the Ag-NPs rather than the interface between ZnO and SiO$_2$ layers itself. Figure 2(d) shows that a linear relationship between $\Delta V_{T}$ and $V_{GO}$ can be established, which is in fact equivalent to the relationship between the number of charges stored in the Ag-NPs per unit area ($=N_q$) and $\Delta V_T$ given by

$$qN_q = C_{SiO_2} \Delta V_{T(hys)}$$

where $C_{SiO_2}$ ($=3.5 \times 10^{-8}$ F/cm$^2$) is the capacitance per unit area of the SiO$_2$ layer and $q$ is the electronic charge. For instance, $\Delta V_{T(hys)}$ of 28.5 V at $V_{GS}$ sweep with $V_{GO}$ of 50 V corresponds to the situation where approximately 6.3 x $10^{11}$/cm$^2$ charges are captured on the Ag-NPs in total. Using $1.4 \times 10^{-11}$/cm$^2$ as the areal density of the Ag-NPs, one can estimate that the average number of charges per Ag-NP is approximately 46. This threshold voltage change and the corresponding number of stored charges per NP are relatively large when compared to conventional MOSFET memory with NPs embedded into gate insulators, but are comparable to those of the memory devices reported by Novembre et al. that are based on pentacene and Au-NPs in a device geometry similar to the devices presented here. The major difference from the conventional devices appears to come from the lack of well-defined tunnel-oxide layer in the present work and Ref. 11.

In order to evaluate the programing ($P$) capability of this ZnO/Ag-NP memory TFT, the shift in threshold voltage $\Delta V_T$ measured with respect to the initial unprogramed value $V_{T(P)}$ was measured as a function of a hold time ($\tau_P$) of the programing pulse of the amplitude $V_{GS}$ of $+40$, $+50$, and $+60$ V, respectively. Subsequently, erasing ($E$) characteristics were measured by monitoring $\Delta V_T$ as a function of a hold time $\tau_E$ for erasing pulse with the amplitudes $V_{GS}$ of $-40$, $-50$, and $-60$ V, respectively. Note that $\Delta V_T$ right before programing and erasing operations are 0 V [$=\Delta V_T(i^{(P)})$] and 17.8 V [$=\Delta V_T(i^{(E)})$], respectively. It is expected that the programing pulse of the positive gate bias will let a portion of the induced electrons be captured at Ag-NPs. Then, those captured electrons will function like interface fixed charges that eventually results in the $V_T$ shift in the positive $V_{GS}$ direction. Upon application of “erasing” pulse of the negative gate bias, some or all of the precaptured electrons will be detrapped, resulting in the $V_T$ shift in the negative $V_{GS}$ direction. [See Fig. 3(a) for the illustration comparing the number of the induced carriers between “programed” and “erased case,” which is directly related to the $V_T$ shift.] As shown in Fig. 3(b), the magnitude of $\Delta V_T(i^{(P)})$ increases with both the pulse duration...
tion $\tau_{PE}$ and the magnitude of $V_G^{(P/E)}$. Note that the difference in $\Delta V_T$ even at the shortest pulse width $\tau_{PE}$ of $10^{-4}$ s is $+5.0/-4.6$ V in average, which is large enough to be sensed. Hence, it may be considered that ZnO/Ag-NP memory TFTs can potentially be used as fast-operating memories.

As another substantial factor that characterizes the non-volatile memory devices, the retention characteristics were studied by measuring $\Delta V_T$ of the device as a function of time after applying a $V_G^{(P/E)}$ stress of $+60/-60$ V for 1 s. The charge retention characteristics shown in Fig. 3(b) indicate that the memory window, that is, a difference in $\Delta V_T$ between the programing and erasing operations, decreases over time, for example, to $27\%$ of the initial value after a period of $10^5$ s. From the extrapolation of the experimental data, it is projected that after programing, the device can retain the initial memory window up to $10^7$ s. This rather rapid decrease in the memory window is mainly attributed to the low energy barrier for charge backflow from Ag-NPs to ZnO. While the difference in energy between the work function of Ag and the conduction band edge of ZnO is only of the order of 0.1 eV, the previous reports indicate that the potential barrier height between the Ag and the ZnO is in the range of 0.8–0.9 eV when they are contacted together. This barrier height would prevent the backflow and provide some retention as shown in this work, but this may be further improved by applying a tunnel-oxide structure similar to Si-based memory devices or by using NPs with a higher work function that can create higher energy barrier for the charge backflow.

In summary, sol-gel ZnO based memory TFTs were fabricated using solution processes with Ag-NPs embedded as charge storage nodes at the insulator-ZnO interface. Pulsed operation indicates that they can be programed or erased to yield measurable threshold voltage shift at a timescale of as short as 0.1 ms. Charge retention characteristics are currently poorer than the established memory technologies, but we believe that a barrier engineering can lead to a further improvement in retention characteristics. With such refinement and development of reliable dielectric technologies that can be prepared by an inexpensive process compatible with various substrates, ZnO-memory TFTs presented here may serve as reliable building blocks for low-cost memory technologies not only in various established applications but also in new emerging systems such as memory-on-panel displays and transparent electronic devices.

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18. Another possibility is that migration of Ag atoms into SiO$_2$ and subsequent creation of deep-level states, which can also function as charge storage nodes. Identification of the exact mechanisms will require further studies such as temperature-dependent measurement. Authors are currently in preparation for such study, and results will be reported elsewhere.