Channel length dependence of hot-carrier-induced degradation in n-type drain extended metal-oxide-semiconductor transistors

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Channel length ($L_{ch}$) dependence of hot-carrier-induced degradation in n-type drain extended metal-oxide-semiconductor (DEMOS) transistors stressed under high drain voltage and high gate voltage is investigated. On-resistance degradation is reduced in longer $L_{ch}$ device, however, threshold voltage shift ($\Delta V_T$) is greater. Charge pumping data reveal that electron trapping in gate oxide above channel region is responsible for $\Delta V_T$. Simulation results show that longer $L_{ch}$ device exhibits enhanced vertical electric field ($E_y$), i.e., enhanced hot-electron injection, in channel region due to the alleviation of Kirk effect. Results presented in this letter reveal that enhanced $\Delta V_T$ driven by enhanced channel $E_y$ may become a serious reliability concern in DEMOS transistors with longer $L_{ch}$. © 2008 American Institute of Physics. [DOI: 10.1063/1.3040693]

Drain extended metal-oxide-semiconductor (DEMOS) transistors are usually used in smart-power applications because they can be easily integrated into standard complementary MOS (CMOS) process. DEMOS transistors are prone to hot-carrier-induced degradation especially for devices operated under high drain voltage ($V_D$) and high gate voltage ($V_G$) because Kirk effect may become significant. It has been reported that devices with significant Kirk effect exhibit serious on-resistance ($R_{on}$) degradation. To suppress Kirk effect for a better reliability, devices using larger layout parameter or higher drift region doping has been proposed. In this letter, the effect of channel length ($L_{ch}$) on hot-carrier-induced degradation in n-type DEMOS device stressed under high $V_D$ and high $V_G$ is investigated. Although $R_{on}$ degradation is reduced in longer $L_{ch}$ device, an unexpected larger positive threshold voltage shift ($\Delta V_T$) is observed. Charge pumping technique and technology computer-aided-design (TCAD) simulations are performed to understand the mechanism responsible for such an anomalous $L_{ch}$ dependence on $\Delta V_T$.

The cross section of n-type DEMOS transistors used in this letter is shown in the inset of Fig. 1. This device is fabricated with a modified 0.25 μm CMOS process. $L_{ch}$ of the device with the same doping profile are 1.4, 2.5, and 4 μm (mask drawn length). The operational voltage is 20 V for both $V_D$ and $V_G$. To ensure a reliable operation under $V_D=20$ V, a high quality gate oxide with 50 nm thickness is grown by thermal oxidation method for all $L_{ch}$ devices. $R_{on}$ ($=V_D/I_D$, where $I_D$ is drain current) measured at $V_G=0.1$ V and $V_D=20$ V are 14, 29, and 56 mΩ mm² for $L_{ch}=1.4, 2.5$, and 4 μm devices, respectively. Threshold voltage ($V_T$) extracted by constant current method at $V_D=0.1$ V is roughly 1 V for all $L_{ch}$ devices. dc hot-carrier stressing is performed at room temperature with the source and bulk connected to ground. Charge pumping technique is carried out to examine the formation of interface state ($\Delta N_{it}$) and oxide trap ($\Delta N_{ot}$) in channel region during stressing. The pulse with high level fixed at 4 V and low level ($V_{gl}$) varied from −0.4 to 2 V is applied to the gate under a frequency of 500 kHz. To investigate hot-carrier-induced damage located in the channel region, charge pumping current ($I_{cp}$) is measured at source terminal while drain is floating. The stress tests are interrupted periodically to measure the degradation of device parameters (including $R_{on}$ and $V_T$) and $I_{cp}$. TCAD simulations (using ATLAS device simulator) are also performed to investigate the degradation mechanism for devices with different $L_{ch}$.

Figure 1 shows bulk current ($I_B$) versus $V_G$ characteristics at $V_D=22$ V and gate current ($I_G$) versus $V_G$ characteristics at $V_D=0$ V for devices with various $L_{ch}$. From $I_B$ data, the small $I_G$ (<10⁻¹² A/μm) indicates that gate current injection at source side region is negligible and 50 nm gate oxide is thick enough for $V_{gl}=20$ V operation. From $I_B$ data, two $I_G$ peaks are exhibited in $L_{ch}=1.4$ μm device, while only one $I_G$ maximum is seen in $L_{ch}=4$ μm device. Simulated impact ionization (II) and potential contours at $V_D=22$ V and $V_G=20$ V in $L_{ch}=1.4$ and 4 μm devices are shown in

FIG. 1. (Color online) $I_B$ vs $V_G$ characteristics at $V_D=22$ V and $I_G$ vs $V_G$ characteristics at $V_D=0$ V for devices with various $L_{ch}$. The schematic cross section of the n-type DEMOS transistor used in this letter is shown in the inset.
Figs. 2(a) and 2(b), respectively. The simulations are well calibrated according to measured $I_p-V_g$ data. Compared with $L_{ch}=4$ μm device, the magnitude of II rate is greater and the location of II peak is right shifted toward $N^+$ drain in $L_{ch}=1.4$ μm device. Results in Fig. 1 indicate that Kirk effect (related to the parasitic n-p-n bipolar transistor as illustrated in Fig. 1) is significant in $L_{ch}=1.4$ μm device, while Kirk effect is alleviated in $L_{ch}=4$ μm device due to a lower current density in $N^+$ drift region. In our stress tests, devices are stressed under $V_{ds}=22$ V with various $V_g$ (5–20 V). Because the $V_g$ to produce the most device degradation is $V_g=20$ V, the following analysis is focused on devices stressed under $V_g=20$ V. Figure 3 shows $\Delta V_T$ and $R_{on}$ degradation (inset) for devices with various $L_{ch}$. The smaller $R_{on}$ degradation in longer $L_{ch}$ device can be explained by the alleviation of Kirk effect. Because $R_{on}$ degradation is mainly determined by damage in $N^+$ drift region rather than damage in channel region, the alleviation of Kirk effect produces less damage in drift region, leading to smaller $R_{on}$ degradation. However, the device with longer $L_{ch}$ produces greater $\Delta V_T$, though the magnitude of II rate in the channel region is smaller as seen in Fig. 2(a).

To investigate the mechanism responsible for the anomalous $L_{ch}$ dependence on $\Delta V_T$, $I_{cp}$ resulted from damage located in the channel region is examined. The fresh and aged $I_{cp}$ in $L_{ch}=1.4$ and 4 μm devices are shown in Figs. 4(a) and 4(b), respectively. No apparent lateral shift in $I_{cp}$ spectrum (i.e., small $\Delta N_{ot}$) after stressing is observed in $L_{ch}=1.4$ μm device. However, a significant rightward shift as a function of time in $I_{cp}$ spectrum (i.e., significant negative $\Delta N_{ot}$) after stressing is observed in $L_{ch}=4$ μm device. Note that the doping profile in channel region is almost uniform, revealing that the rightward shift in $I_{cp}$ spectrum is not caused by doping profile variation. To evaluate hot-carrier-induced $\Delta N_{ot}$ in $L_{ch}=4$ μm device, the impact of $\Delta N_{ot}$ on $I_{cp}$ spectrum should be eliminated. This can be achieved by a properly leftward shift of $I_{cp}$ spectrum by the amount of flat-band voltage ($V_{fb}$) shift. $V_{fb}$ is defined as the $V_g$ when hole concentration at Si/SiO$_2$ interface reaches $10^{14}$ cm$^{-3}$. From simulation results, the fresh $V_{fb}$ in channel region is roughly −0.4 V. The resulting $I_{cp}$ due to $\Delta N_{ot}$ only is shown in the inset of Fig. 4(b). $I_{cp}$ increase due to $\Delta N_{ot}$ is much greater in $L_{ch}=1.4$ μm device [Fig. 4(b)] than that in $L_{ch}=4$ μm device [inset of Fig. 4(b)]. This is consistent with results in Fig. 2(a) that II rate in channel region is much greater in $L_{ch}=1.4$ μm device. From data in Figs. 4(a) and 4(b), it is suggested that significant $\Delta V_T$ in $L_{ch}=4$ μm device is mainly resulted from severe electron trapping in gate oxide above channel region.

To identify the driving force of electron trapping, Fig. 5 shows simulated vertical electric field ($E_z$) distribution along channel at Si/SiO$_2$ interface [cutline is indicated in Fig. 2(b)].
under $V_d = 22$ V and $V_g = 20$ V. $E_y$ is much higher in $L_{ch} = 4 \ \mu m$ device than that in $L_{ch} = 1.4 \ \mu m$ device, indicating that hot-electron injection and trapping is enhanced in $L_{ch} = 4 \ \mu m$ device. Such a result explains why greater $\Delta V_T$ is exhibited in longer $L_{ch}$ device. To explain such $L_{ch}$ dependence on $E_y$ (related to $\Delta N_{ot}$), potential contours of the devices are analyzed in Fig. 2(b). It is clear that a relatively large portion of potential drop is distributed in $N^-$ drift region in $L_{ch} = 1.4 \ \mu m$ device due to significant Kirk effect, resulting in smaller $E_y$ near the gate oxide in channel region. On the other hand, relatively large portion of potential drop (especially in vertical direction) is distributed in channel region in $L_{ch} = 4 \ \mu m$ device due to the alleviation of Kirk effect, resulting in higher $E_y$ near the gate oxide. Note that the peak $E_y$ is located in drain side of channel region (in Fig. 5), indicating that $\Delta V_T$ is caused by $\Delta N_{ot}$ in the gate oxide above the drain side of channel region. $I_g$ data in Fig. 1 also reveal that source-side gate current injection is negligible at $V_g = 20$ V. Such a result is quite different from recently published data that significant $\Delta V_T$ is due to source-side injection.\textsuperscript{10} From the above analysis, it is suggested that the greater $\Delta V_T$ in longer $L_{ch}$ device is resulted from severe hot-electron injection and trapping caused by enhanced $E_y$ in drain side of channel region.

In this letter, hot-carrier-induced $R_{on}$ degradation is reduced but $\Delta V_T$ is greater in $n$-type DEMOS device with longer $L_{ch}$. The greater $\Delta V_T$ in longer $L_{ch}$ device is attributed to enhanced hot-electron injection and trapping in gate oxide above channel region. The enhanced electron injection is resulted from enhanced $E_y$ in drain side of the channel region because of the alleviation of Kirk effect. Results presented in this study suggest that enhanced $\Delta V_T$ driven by enhanced channel $E_y$ in longer $L_{ch}$ device should be noticed in evaluating the reliability of DEMOS devices.

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